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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,961	06/05/2000	Akihiko Ohwada	1341.1048/JDH	8507

21171 7590 11/02/2005

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EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,961	OHWADA, AKIHIKO	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11-30 have been considered. Claims 11, 19, 23 and 27-30 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as field 24 August 2005 and Amendment as filed 24 August 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 28, 29, and 30 are rejected under 35 U.S.C. 102(e) as being taught by Krygowski et al., U.S. Patent Number 6,049,860 (herein referred to as Krygowski).

5. Referring to claim 28, Krygowski has taught a processor execution pipeline method, comprising:

a. Decoding a first instruction into a first control signal, and decoding all other instructions with the exception of the first instruction into a second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. Performing a first operation on a first data when receiving the first control signal, and passing the first data when receiving the second control signal via a first processing unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. Decoding a second instruction into a third control signal, and decoding all other instructions with the exception of the second instruction into a fourth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. Performing a second operation on a second data via a second processing unit when receiving the second control signal, where the second data is an output of the first processing unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

e. Selecting an output of the second processing unit or the second data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6),

f. Wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through to a next stage (Krygowski column 1, lines 13-38; column 1, line

61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

6. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

7. Referring to claim 29, Krygowski has taught a processor execution pipeline method, comprising:

a. Decoding a first instruction into a first control signal and all other instructions into a second control signal, and decoding a second instruction into a third control signal and all other instructions with the exception of the second instruction into a fourth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

b. First and second processing units respectively executing first and second instructions using data held in a latching unit, wherein each instruction is decoded to pass the data held in the latching unit through the first processing unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column

3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6),

c. And the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through to a next stage (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

8. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

9. Referring to claim 30, Krygowski has taught a processor execution pipeline method, comprising:

a. Decoding a first instruction in a first processing stage into a first control signal, and decoding all other instructions with the exception of the first instruction into a second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. Decoding a second instruction in a second processing stage into a third control signal, and decoding all other instructions with the exception of the second instruction into a fourth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. Executing a first operation on a first data upon receipt of the first control signal, and holding a result of the execution of the first operation until receipt of the second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. Executing a second operation on the result of the execution of the first operation when receiving the third control signal and holding a result of the execution of the second operation until receipt of the fourth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

e. Selecting the result of the first operation or the second operation as an output, where the first instruction and the second instruction are unrelated to one another (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6),

f. Wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through to a next stage (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

10. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 11-27 are rejected under 35 U.S.C. 103(a) as being taught by Krygowski et al., U.S. Patent Number 6,049,860 (herein referred to as Krygowski) in view of Texas Instruments's Semiconductor Service Support (herein referred to as TI).

13. Referring to claim 11, Krygowski has taught a processor execution pipeline, comprising:

a. A unit that determines at least a kind of instruction, decodes a first instruction into a first control signal, and decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. A first processing unit that performs a first operation on a first data when receiving the first control signal, and passes through the first data when receiving the second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. A unit that determines at least a kind of instruction, decodes a second instruction into a third control signal, and decodes all other instructions with the exception of the second instruction into a fourth control signal upon determining at least the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. A second processing unit that performs a second operation on a second data when receiving the third control signal, the second data being an output of the first processing unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

e. A multiplexer that selects an output of the second processing unit or the second data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6),

f. Wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

14. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). Krygowski has not explicitly taught a first instruction decoding unit and a second instruction decoding unit. However, Krygowski insinuates that there is some type of control system which generates control signals to determine when instructions move from stage to stage and when a stage is bypassed (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). TI has taught that a decoder simply converts information into a format more readily

understood by the system (TI term "Decoder"). A person of ordinary skill in the art at the time the invention was made would have recognized that a decoder generates control signals from the instructions understood and usable by the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the decoder of TI in the device of Krygowski.

15. Referring to claim 12, Krygowski has taught wherein the multiplexer selects an output of the second processing unit when receiving the third control signal, and selects the second data when receiving the fourth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

16. Referring to claim 13, Krygowski has taught a latching unit that holds the output of the first processing unit where the second data is data held by the latching unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). In regards to Krygowski, the pipe stages registers are latches, since they store data. See the definition of latch from FOLDOC provided in previous actions.

17. Referring to claim 14, Krygowski has taught wherein the first processing unit receives multiple data as the first data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

18. Referring to claim 15, Krygowski has taught a processor execution pipeline, comprising:

a. A unit that determines at least a kind of instruction, decodes a first instruction into a first control signal, and decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. A first processing unit that performs a first operation on a first data when receiving the first control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. A multiplexer that selects an output of the first processing unit or the first data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. A unit that determines at least a kind of instruction, decodes a second instruction into a third control signal, and decodes all other instructions with the exception of the second instruction into a fourth control signal upon determining at leas the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

e. A second processing unit that performs a second operation on a second data when receiving the third control signal, and passes the second data when receiving the

fourth control signal, where the second data is an output of the multiplexer (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

19. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). Krygowski has not explicitly taught a first instruction decoding unit and a second instruction decoding unit. However, Krygowski insinuates that there is some type of control system which generates control signals to determine when instructions move from stage to stage and when a stage is bypassed (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). TI has taught that a decoder simply converts information into a format more readily understood by the system (TI term "Decoder"). A person of ordinary skill in the art at the time the invention was made would have recognized that a decoder generates control signals from the instructions understood and usable by the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the decoder of TI in the device of Krygowski.

20. Referring to claim 16, Krygowski has taught wherein the multiplexer selects an output of the first processing unit when receiving the first control signal, and selects the first data when receiving the second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

21. Referring to claim 17, Krygowski has taught a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). In regards to Krygowski, the pipe stages registers are latches, since they store data. See the definition of latch from FOLDOC provided in previous actions.

22. Referring to claim 18, Krygowski has taught wherein the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

23. Referring to claim 19, Krygowski has taught a processor execution pipeline, comprising:

a. A unit that determines at least a kind of instruction, decodes a first instruction into a first control signal, and decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line

3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. A first processing unit that performs a first operation on a first data when receiving the first control signal, and passes the first data when receiving the second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. A unit that determines at least a kind of instruction, decodes the first instruction into a third control signal, decodes a second instruction into a fourth control signal, and decodes all other instructions with the exception of the first and second instructions into a fifth control signal upon determining at least the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. A second processing unit that performs a second operation on a second data when receiving the third control signal, and performs a third operation on the second data when receiving the fourth control signal, where the second data is an output of the first processing unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

e. A multiplexer that selects an output of the second processing unit or the second data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3;

column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6),

f. Wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

24. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). Krygowski has not explicitly taught a first instruction decoding unit and a second instruction decoding unit. However, Krygowski insinuates that there is some type of control system which generates control signals to determine when instructions move from stage to stage and when a stage is bypassed (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). TI has taught that a decoder simply converts information into a format more readily understood by the system (TI term "Decoder"). A person of ordinary skill in the art at the time the invention was made would have recognized that a decoder generates control signals from the

instructions understood and usable by the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the decoder of TI in the device of Krygowski.

25. Referring to claim 20, Krygowski has taught wherein the multiplexer selects an output of the second processing unit when receiving either one of the third or the fourth control signals, and selects the second data when receiving the fifth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

26. Referring to claim 21, Krygowski has taught a latching unit that holds the output of the first processing unit, where the second data is data held by the latching unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). In regards to Krygowski, the pipe stages registers are latches, since they store data. See the definition of latch from FOLDOC provided in previous actions.

27. Referring to claim 22, Krygowski has taught wherein the first processing unit receives multiple data as the first data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

28. Referring to claim 23, Krygowski has taught a processor execution pipeline, comprising:

a. A unit that determines at least a kind of instruction, decodes a first instruction into a first control signal, decodes a second instruction into a second control signal, and decodes all other instructions with the exception of the first and second

instructions into a third control signal upon determining at least the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. A first processing unit that performs a first operation on a first data when receiving the first control signal, and performs a second operation on the first data when receiving the second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. A multiplexer that selects an output of the first processing unit or the first data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. A decoding unit that decodes the first instruction into a fourth control signal, and decodes all other instructions with the exception of the first instruction into a fifth control signal upon determining at leas the kind of instruction (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

e. A second processing unit that performs a third operation on a second data when receiving the fourth control signal, and passes the second data when receiving the fifth control signal, where the second data is an output of the multiplexer

(Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6),

f. Wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

29. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). Krygowski has not explicitly taught a first instruction decoding unit and a second instruction decoding unit. However, Krygowski insinuates that there is some type of control system which generates control signals to determine when instructions move from stage to stage and when a stage is bypassed (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). TI has taught that a decoder simply converts information into a format more readily understood by the system (TI term "Decoder"). A person of ordinary skill in the art at the time

the invention was made would have recognized that a decoder generates control signals from the instructions understood and usable by the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the decoder of TI in the device of Krygowski.

30. Referring to claim 24, Krygowski has taught wherein the multiplexer selects an output of the first processing unit when receiving either one of the first or the second control signals, and selects the first data when receiving the third control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

31. Referring to claim 25, Krygowski has taught a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). In regards to Krygowski, the pipe stages registers are latches, since they store data. See the definition of latch from FOLDOC provided in previous actions.

32. Referring to claim 26, Krygowski has taught wherein the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

33. Referring to claim 27, Krygowski has taught a processor execution pipeline having at least a latching unit to hold and output data, comprising:

a. A unit to convert a first instruction into a first control signal, and to convert all other instructions with the exception of the first instruction into a second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

b. A first processing unit to perform a first operation on a first data when receiving the first control signal, and to pass the first data when receiving the second control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

c. A unit to convert a second instruction into a third control signal, and to convert all other instructions with the exception of the second instruction into a fourth control signal (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

d. A second processing unit to perform a second operation on a second data when receiving the third control signal where the second data is an output of the first processing unit (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6); and

e. A multiplexer that selects an output of the second processing unit or the second data (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3;

column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6);

f. Wherein the latching unit holds an output of the first processing unit and the second data is held by the latching unit allowing the latching unit to be shared by the first a second processing units (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). In regards to Krygowski, the pipe stages registers are latches, since they store data. See the definition of latch from FOLDOC provided in previous actions,

g. And the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6).

34. In regards to Krygowski, there is some type of control that determines when an instruction enters a pipeline stage and determines when to bypass a stage based upon generated control signals, i.e. when the instruction is a store type instruction, the computation stages of the pipeline are bypassed based upon the control signals from the control unit, which receives the instructions and converts the instructions into the correct control signals (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). Krygowski has not explicitly taught a first instruction decoding unit and a second instruction decoding unit.

However, Krygowski insinuates that there is some type of control system which generates control signals to determine when instructions move from stage to stage and when a stage is bypassed (Krygowski column 1, lines 13-38; column 1, line 61 to column 2, line 3; column 3, lines 8-27; column 3, line 49 to column 4, line 34; Figure 2; Figure 3; Figure 4; Figure 5; and Figure 6). TI has taught that a decoder simply converts information into a format more readily understood by the system (TI term "Decoder"). A person of ordinary skill in the art at the time the invention was made would have recognized that a decoder generates control signals from the instructions understood and usable by the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the decoder of TI in the device of Krygowski.

Response to Arguments

35. Examiner notes that Applicant's arguments indicates on pages 8 and 9 that independent claim 15 was amended, however, the listing of claims has labeled claim 15 as "previously presented" and no marks showing changes to the text are present. Therefore, claim 15 was considered as currently presented without any amendments made to it.

36. Applicant's arguments filed 24 August 2005 have been fully considered but they are not persuasive. Applicant argues in essence on pages 8-9

> Unlike the Krygowski system for processing floating point store instructions in a floating point pipeline directed to improving data dependency..., according to the processor execution pipeline of the present invention, "the first, second and all other instructions are selectively decoded based on whether operations are to be

performed thereto in a current processing stage or passed through data to a next stage".

37. This has not been found persuasive. The newly added claim limitation to the independent claims essentially repeat what was claimed in more detail in the independent claims. For example, with claim 28, the claim recites the limitations "decoding a first instruction into a first control signal, and decoding all other instructions with the exception of the first instruction into a second control signal" and "a second instruction decoding unit to convert a second instruction into a third control signal, and to convert all other instructions with the exception of the second instruction into a fourth control signal". This meets the new limitation of "the first, second and all other instructions are selectively decoded", since the first and second instruction decoder decodes the first and second instructions into different signals that the decoder selects. The claim then recites a first processing unit and a second processing unit that performs operations or passes the operation through the processing unit based upon the signals from the first and second decoders, which is similar to the new limitation "based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage." Since the signals produced by the decoders determines what the processing unit does with the instruction, that means that the decoders select the signals based upon whether an operation is to be done or the data passed through. Therefore, as shown in the rejection above, Krygowski still reads upon the claim, since the scope of the claim has not been effectively changed.

38. Applicant argues in essence on page 8

> ...the present invention selectively decodes or converts instructions for performing operations in a current processing stage or for passing through data to a next stage without requiring a holding circuit for holding the data to be passed through.

39. This has not been found persuasive. This has not been claimed. The claims do not contain the limitation of the latches, as other claims do, but this does not mean that, simply because a limitation is omitted, that the element is no longer present within the invention. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., passing through data to a next stage without requiring a holding circuit) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Also, this assertion is not evident or taught within Applicant's specification. For example, all drawings show stage latch circuits for holding data between stages even for pass through data..

Conclusion

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

41. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

42. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
27 October 2005

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